

Modification of Simulation Conversion Assembly for Support of Voyager Project and Pioneer-Venus 1978 Project

S. H. Yee

DSN Data Systems Section

The Simulation Conversion Assembly (SCA) has been upgraded to provide the additional capabilities of simulating Voyager and Pioneer-Venus 1978 telemetry data streams for verifying the integrity of the Deep Space Stations while continuing to fulfill the DSN test and training support requirements. A summary of the requirements and the implementations are presented in this article.

I. Introduction

The Simulation Conversion Assembly (SCA), as part of the DSS Test and Training Subsystem, has been upgraded to provide the additional hardware and software capabilities listed below to support Voyager and Pioneer-Venus 1978 (PV-78) Projects:

- (1) Voyager short constraint length convolutional coding.
- (2) PV long constraint length convolutional coding.
- (3) Voyager project data patterns.
- (4) Pioneer-Venus 1978 project data patterns.

The SCA consists of two levels of capability to support the respective telemetry data processing equipment at each of the deep space stations.

- (1) SCA provides four telemetry data channels, required at the 26-m stations.
- (2) SCA provides six telemetry data channels, required at the 64-m stations.

The SCA described in this article is the six-channel configuration for the 64-m stations.

II. New Hardware Capabilities

A. Voyager Short Constraint Length Convolutional Coder

The SCA is required to provide nonsystematic convolutional coding with constraint length of 7 bits at the computer-controlled code format of 1/2 and 1/3 on three data channels

for symbol rates up to 230,400 bits/second. The Voyager coding connection vector will be as shown in Figs. 1 and 2.

B. PV-78 Long Constraint Length Convolutional Coder

The SCA is required to provide nonsystematic convolutional coding with constraint length of 32 bits at the computer-controlled code format of 1/2 on three data channels for symbol rates up to 2048 bits/second. The PV-78 coding connection vectors will be as shown in Fig. 3. Thirty-two bits of tail code are inserted, and the register is reset at the end of each frame in both the manual and computer modes of operation.

III. New Software Capabilities

A. Voyager Project Data Patterns

Software-generated, framed-synchronized data patterns are provided to simulate the Voyager formats and frame sizes. An incrementing data pattern of nine different frame sizes as shown in Fig. 4 is required for data rates up to 115.2 kbytes/second, in addition to the incrementing pattern. Fixed, static data of seven different frame sizes is required for data rates up to 7200 bits/second as shown in Fig. 5.

B. PV-78 Data Pattern

Software-generated, frame synchronized data patterns representing Pioneer-Venus formats are provided for each of the SCA channels having long constraint length convolutional coding capability. All Pioneer-Venus frames are 512 bits in length; each frame corresponds to an encoding cycle. The frame count in the orbiter and bus data patterns are incremented one count per frame as shown in Fig. 6. The probe patterns are static as shown in Fig. 7.

Provision is made for operator-entry changes to the format identification (ID) in bus and orbiter patterns, the probe ID in probe pattern, the data rate ID in any type pattern, and any computer word in the data-generating table.

C. High-Speed and Wideband Input and Output

The SCA processes a 56-kbit/second (kbs) wideband input of 4800-bit block size, with output data rate up to 44.8 kbs on one channel, and simultaneously processes a 7.2-kbs high-speed input of 1200-bit block size with an output rate up to 40 bits/second on a second channel.

IV. Hardware Implementation

To provide for the additional convolutional coding function, the SCA required the addition of the new convolutional coder drawer (CCD). The new CCD contains all necessary hardware to enable the SCA to provide the capabilities defined in Paragraph II. The CCD consists of four major functions. See Fig. 8 for block diagram of CCD.

A. Convolutional Coding Section

There are four modes of convolutional coding:

- (1) Systematic 1/2 (S 1/2).
- (2) Nonsystematic 1/2 (\bar{S} 1/2).
- (3) Systematic 1/3 (S 1/3)
- (4) Nonsystematic 1/3 (\bar{S} 1/3)

When S 1/2 or \bar{S} 1/2 is selected, the output consists of two symbols for each data bit. The coders are also able to operate in an uncoded mode. The modes of operation are described below:

- (1) S 1/2: In the S 1/2 mode, the first output symbol is the true data bit, and the other is parity symbol. Example:

$$P_{1N}D_N \cdots P_{12}D_2P_{11}D_1$$

where D_N is the first data bit and P_{1N} is the first parity bit.

- (2) \bar{S} 1/2: In the \bar{S} 1/2 mode, the two output symbols are both parity symbols. Example:

$$P_{2N}P_{1N} \cdots P_{22}P_{12}P_{21}P_{11}$$

where P_{2N} and P_{1N} are parity bits.

- (3) S 1/3: In the S 1/3 mode, the first output symbol is the true data bit; the other two symbols are parity symbols. Example:

$$P_{2N}P_{1N}D_N \cdots P_{22}P_{12}D_2P_{21}P_{11}D_1$$

where D_N is the first data bit, P_{1N} is the first parity bit and P_{2N} is the second parity bit.

- (4) $\overline{S} 1/3$: In the $\overline{S} 1/3$ mode, all three output symbols are parity symbols. Example:

$$P_{3N} P_{2N} P_{1N} \cdots P_{32} P_{22} P_{12} P_{31} P_{21} P_{11}$$

B. Timing Section

This section provides the control to synchronize the data generated from the computer and resets the register at the end of each frame. It also provides the clock signals to the data generator to code the data at the rates of 1/2 or 1/3 format.

C. Computer Control

The computer control section provides the means for the computer to control and monitor the coder.

D. Selection Matrix

The CCD is required to have manual control of the convolutional error rate (CER) selection and routing for assemblies in the DSS.

V. Software Implementation

The new program is a modification of the current program. The code that pertains only to the Viking mission has been deleted from the current program to make core space available for the new code to meet the requirements defined in Paragraph III. All of the required mission-independent functions of the current program have been retained. The additions to the program provide SCA capabilities to support the DSS test and training activities for the Voyager and PV-78 missions. The program will support both stand-alone and long-loop operations at all stations. Stand-alone data streams with incrementing counters will be output at selected rates up to 115,200 bits/second. Long-loop data will be received on both wideband and high-speed lines and routed to selected output channels. The program allows for the altering of fixed and incrementing data tables, provides for controlling the new convolutional coders, and for the selecting of fixed data patterns.

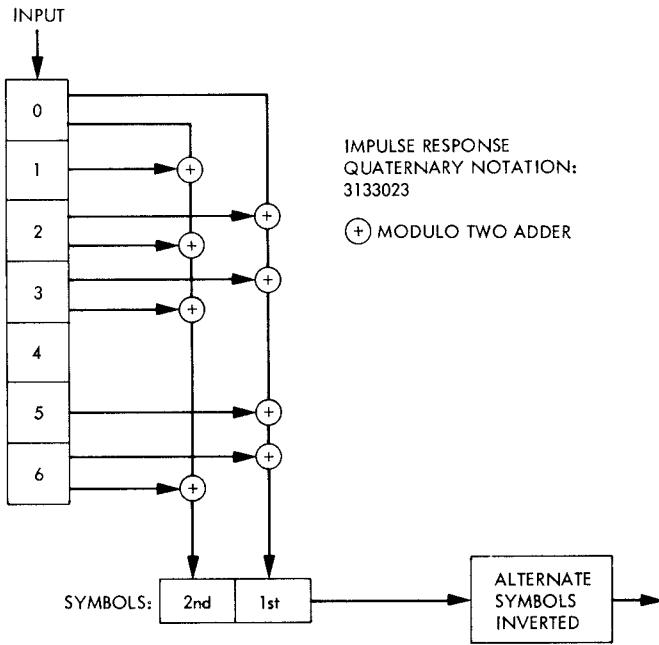


Fig. 1. Schematic of Voyager connection vector, constraint length = 7, rate = $\frac{1}{2}$

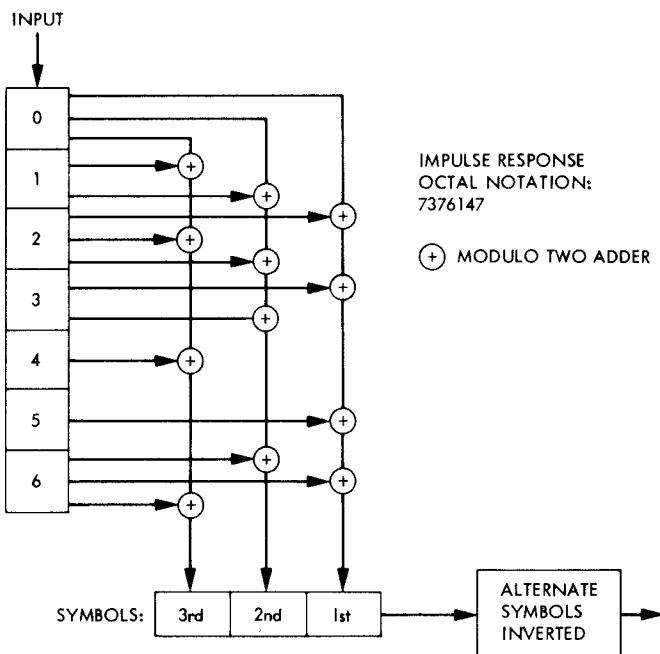


Fig. 2. Schematic of connection vector, constraint length = 7, rate = $\frac{1}{3}$

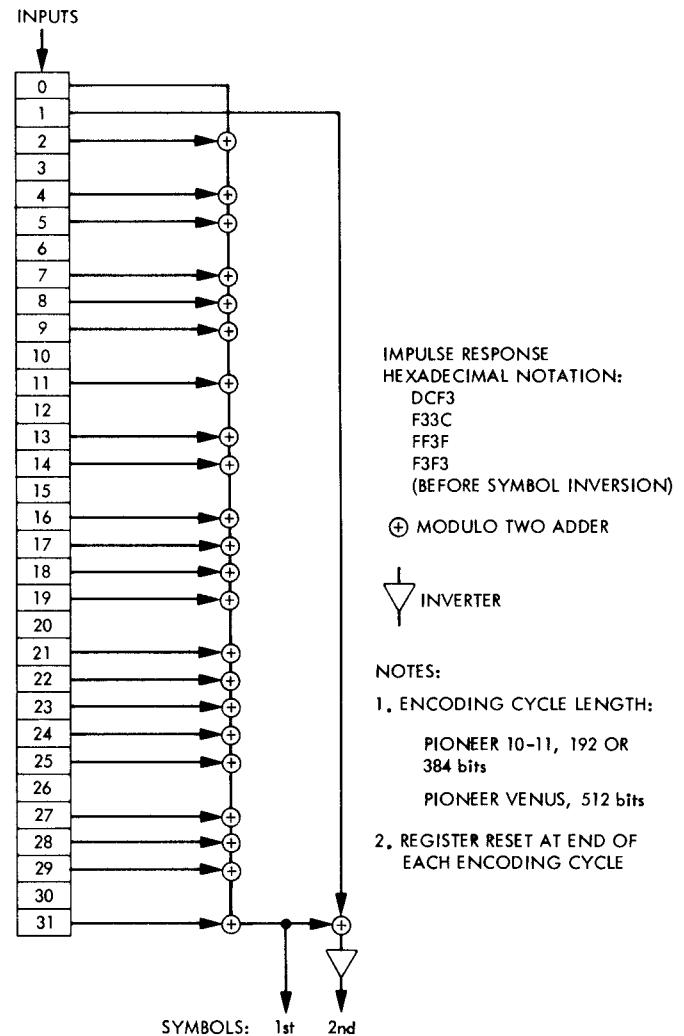


Fig. 3. Schematic of PV-78 connection vector, constraint length = 32, rate = $\frac{1}{2}$

VOYAGER INCREMENTING DATA PATTERN (288 WORDS)

Want

- 1) Format 10: Set by mnemonic input.
 - 2) Frame sizes (20, 48, 64, 112, 120, 168, 180, 224, and 288 words) set by mnemonic input.
 - 3) See SOM-DYS-5128, Section 5.7 for Voyager mnemonic codes.
 - 4) Picture Count Increments from 0 to 59 at a rate of one count per 800 Line Counts.
 - 5) Line Count increments from 1 to 800 at a rate of one count per frame.
 - 6) Generator word No. 19 provides recycle of word No. 3 picture and line count.
 - 7) Applicable to SCA output channels as follows:
 - 8) Convolutional coded: Channels 1, 2, or 5.

Fig. 4. Voyager incrementing data format

VOYAGER FIXED DATA PATTERN (180 WORDS)

Generator Word No.	Times Output	Buffer Word No.	Format	Binary Contents - - - - -								Octal	Hex	
				0	1	2	3	-	-	-	-			
1	1	1	[Frame Sync]	0	0	0	0	1	1	0	0	1	1	0
2	1	2	[Format ID] [Time Subcon]	1	1	0	1	0	1	1	1	0	1	1
3	1	3	Mod 60 Count [Mod 800 Count]	0	1	0	1	0	1	0	0	0	0	17
4	33	4-36	DATA (177 24-Bit Words) —	0	1	0	1	0	1	0	1	0	1	D3000F
5	36	37-72	DATA (177 24-Bit Words) —	1	0	1	0	1	0	1	0	1	0	5A0155
6	36	73-108	DATA (177 24-Bit Words) —	1	1	0	0	1	0	0	1	1	0	25000325
7	36	109-144	DATA (177 24-Bit Words) —	0	0	1	1	0	0	1	1	0	1	25252525
8	36	145-180	DATA (177 24-Bit Words) —	0	1	0	1	0	1	0	1	0	1	555555

Notes:

- 1) Format ID = Set by mnemonic input.
- 2) Frame Sizes (20, 48, 64, 112, 120, 168, 180 words) set by mnemonic input.
- 3) See SOM-DVS-5128, section 5.7 for Voyager mnemonic codes.
- 4) Applicable to SCA output channels as follows:
 Convolutional coded: Channels 1, 2, and 5.
 Uncoded: Channels 1, 2, 5, and 6.

Fig. 5. Voyager fixed data format

PIONEER - VENUS '78 BUS AND ORBITER INCREMENTING PATTERN (64 WORDS)									
Generator Word No.	Times Output	Buffer Word No.	Format			Binary Contents			Bus Counter
			0	1	2	3	4	-	
1	1	1	[Format ID [Rate 10] [DAS Mode ID [SID [Frame Count]]]	x	x	x	x	x	00125200
2	1	2	Subcom Data [0	0	0	1	0	00AA00
3	18	3-20	Data [0	0	0	0	1	111C7
4	1	21	[Tail] Code Sync [0	0	0	1	1	070707
5	1	22	[Format ID [Rate 10] [DAS Mode ID [0	1	0	0	1	0714305
6	1	23	SID [Frame Count [Subcom Data [x	x	x	x	x	1CF8C5
7	18	24-41	Data [1	0	0	1	0	00AA
8	1	42	[Tail] Code Sync [1	0	0	0	1	01B871
9	1	43	[Format ID [Rate 10] [1	1	0	0	1	22200252
10	1	44	DAS Mode ID [SID [Frame Count [Subcom Data [1	0	1	0	1	4900AA
11	19	45-63	Data [0	1	1	1	0	00AA
12	1	64	[Tail] Code Sync [1	1	1	1	0	00AA

Notes:

- 1) Format and Rate IDs set by mnemonic input. See SCM-DYS-5128, section 5.7 for PVB and PVS mnemonic codes.
- 2) SID = Spacecraft ID: Bus (PVB) = 00₂; Orbiter (PVS) = 10₂.
- 3) Orbiter and Bus patterns can run simultaneously at different data rates.
- 4) Frame Count increments from 0 to 63 at a rate of one increment per 512-bit frame.
- 5) Applicable to SCA output channels as follows:
 Convolutional coded: Channels 1 and 2 or 5.
 Uncoded: Channels 1 and 2, or 5 and 6.

Fig. 6. PVB and PVS incrementing data format

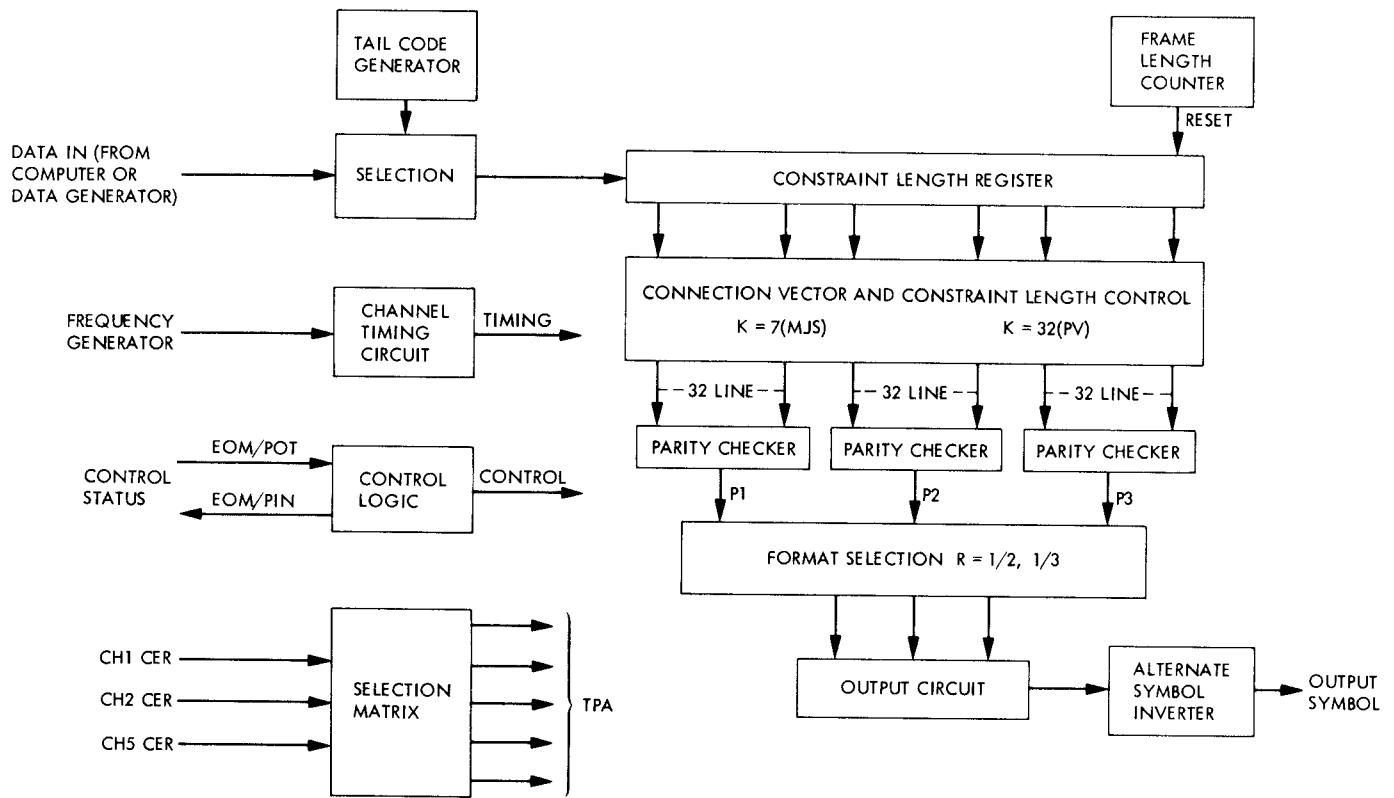


Fig. 8. Voyager/PV-78 DSS Simulation Conversion Assembly convolutional coder block diagram